Amendments to the Claims:

Please amend the claims to read as follows:

1. (Currently amended) An integrated memory device that comprises:
a nonvolatile memory array; and
a nonvolatile buffered memory interface integrated on a substrate with said nonvolatile memory array, wherein the memory interface comprises:
one or more volatile buffers configured to buffer data for read operations directed to the integrated memory device; and
a table memory configured to ~~indicate one or more~~ identify addresses within the nonvolatile memory array that have been recently accessed.

2. (Original) The device of claim 1, wherein the table memory is volatile, and wherein the memory interface is configured to preserve contents of the table memory in nonvolatile memory during absences of electrical power.

3. (Original) The device of claim 2, wherein the memory interface is further configured to restore the contents of table memory from the nonvolatile memory when electrical power returns.

4. (Original) The device of claim 1, wherein when electrical power returns, the memory interface is further configured to restore the one or more volatile buffers to a state preceding the absence of electrical power.

5. (Currently amended) The device of claim 1, wherein the one or more volatile buffers comprise:

a plurality of read buffers each associated with a different region of the nonvolatile memory array and configured to buffer only a subset of data in the associated region for read operations on that ~~the associated~~ region.

6. (Original) The device of claim 1, wherein the memory array comprises magnetic random access memory (MRAM) cells.

7. (Currently amended) An integrated memory device that comprises:

a nonvolatile memory array; and

a nonvolatile buffered memory interface integrated on a substrate with said nonvolatile memory array, wherein the memory interface comprises:

one or more volatile buffers configured to buffer data for read ~~operations~~ commands directed to the integrated memory device; ~~and~~

a table memory configured to ~~indicate one or more~~ identify nonvolatile memory addresses associated with data buffered in the one or more volatile buffers; and

~~wherein the memory interface further comprises:~~

an interface control module that is configured to receive read commands specifying a memory address, wherein the interface control module is coupled to the memory array to conduct read operations to satisfy the read commands and to prepare read buffers to satisfy anticipated read commands, wherein the interface control module is further configured to update the table memory in response to the read commands.

8. (Original) The device of claim 7, further comprising:
an error correction code (ECC) decoder coupled between the memory array and the one or more volatile buffers.

9. (Canceled).

10. (Currently amended) A method of providing access to stored data, the method comprising:
receiving a read command that comprises a read address;
determining whether data from the read address is buffered in a volatile read buffer;
retrieving data from a location in a nonvolatile memory array associated with the read address if the data is not buffered, and buffering the retrieved data in the volatile read buffer;
responding to the read command with data from the volatile read buffers if the data is buffered;
detecting a pending power-down;
storing in nonvolatile memory the read address for data buffered in the volatile read buffer; and
~~preserving during an absence of electrical power information indicative of data in one or more read buffers; and~~
restoring the data to the ~~one or more read buffers~~ volatile read buffer when power returns.

~~wherein said preserving comprises:~~
~~detecting a pending power-down;~~
~~for each of the one or more read buffers, storing in nonvolatile memory a starting address of memory blocks that have been recently accessed.~~

11. (Currently amended) The method of claim 10, wherein said restoring comprises ~~for each of the one or more read buffers~~:

accessing the nonvolatile memory to retrieve the ~~starting~~ read address associated with the read buffer; and

filling the read buffer with data from a memory array, beginning with data associated with the ~~starting~~ read address.

12.-14. (Canceled).

15. (Currently amended) A digital device that comprises:

a memory having a buffered memory interface with one or more read buffers; and

a processor coupled to the memory device and configured to retrieve stored information from the memory,

wherein the processor causes the memory to receive a power down command before electrical power is removed from the memory, and wherein the buffered memory interface responsively stores, in a nonvolatile memory, ~~information that represents~~ one or more addresses ~~within the memory~~ of memory locations that have been recently accessed.

16. (Original) The device of claim 15, wherein the memory interface is further configured to reload the one or more read buffers with data in accordance with information from the nonvolatile memory when power returns.

17. (Canceled).

18. (Currently amended) The device of claim 15, wherein the one or more read buffers comprise:

a plurality of read buffers each associated with a different region of the memory and configured to buffer only a subset of data in the associated region for read operations on ~~the associated~~ that region.

19. (Original) The device of claim 18, wherein the memory interface further comprises:

an interface control module that is configured to receive read commands specifying a memory address, wherein the interface control module is coupled to a nonvolatile memory array to conduct read operations to satisfy the read commands and to prepare read buffers to satisfy anticipated read commands; and

wherein the memory further comprises:

an error correction code (ECC) decoder coupled between the nonvolatile memory array and the one or more read buffers.